FIG 6B illustrates processing subsequent to FIG 5 according to an embodiment in which the entire spacer film is subjected to a stress modulation implant;

FIG 7 illustrates processing subsequent to FIG 6A or FIG 6B in which the spacer film is etched to form spacer structures including at least some stress modulated spacer structures;

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FIG 7 illustrates processing subsequent to FIG 6 in which a second portion of the conductive film is implanted with a second dopant;

FIG 8 illustrates processing subsequent to FIG 5 according to an embodiment in which the spacer film is etched prior to any stress modulation;

FIG 9 illustrates processing subsequent to FIG 8 in which the wafer is subjected to a stress modulation implant; and

FIG 10 illustrates processing subsequent to FIG 9 in which source/drain regions are formed in the wafer.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Reference will now be made in detail to the presently preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. It should be noted that the drawings are in simplified form and are not to precise scale. Although the invention herein refers to certain illustrated embodiments, it is to be understood that these embodiments are presented by way of example and not by way of limitation. The intent of the following detailed description is to cover all modifications, alternatives, and equivalents as may fall within the spirit and scope of the invention as defined by the appended claims.

It is to be understood and appreciated that the process steps and structures described herein do not cover a complete process flow for the manufacture of an integrated circuit. The present invention may be practiced in conjunction with various integrated circuit fabrication techniques that are conventionally used in the art, and only so much of the commonly practiced process steps are included herein as are necessary to provide an understanding of the present invention.